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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: James Loran Ball

Attorney Docket No.: ALTRP134/A1466

Application No.: 10/815,478

Examiner: Please assign

Filed: March 31, 2004

Group: 2183

Title: OPTIMIZED PROCESSORS AND INSTRUCTION ALIGNMENT

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on March 28, 2005 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Joyce L. Ferreira

INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. ALTRP134).

Respectfully submitted,
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Form 1449 (Modified) **Information Disclosure Statement By Applicant** (Use Several Sheets if Necessary)	Atty Docket No. ALTRP134/1466 Applicant: James Loran Ball Filing Date March 31, 2004	Application No.: 10/815,478 Group 2183

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A						
	B						
	C						
	D						
	E						
	F						
	G						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	J							
	K							
	L							
	M							
	N							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	O	Linley Gwennap, "Intel Discloses New IA-64 Features Rotating Registers Reduce Code Expansion: Merced Touted for Big Servers" Microdesign Resources, March 8, 1999, Microprocessor Report
	P	Lars T. Hansen, "Larceny Note #6: Larceny on the SPARC" retrieved from www.ccs.neu.edu/home/will/larceny/notes/notes6-sparc.html, May 5, 1998
	Q	MIPS Instruction Reference, retrieved from www.mrc.uidaho.edu/mrc/people/jff/digital/MIPSir.html. updated September 10, 1998
	R	Nikolova et al., "A Compression/Decompression Scheme for Embedded Systems Code", Electronic Systems and Control Division Research 2003, pp. 36-38.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.